FAST IMPLEMENTATION OF A LINEARITY TEST APPROACH FOR HIGH-RESOLUTION ADCS USING NON-LINEAR RAMP SIGNALS

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ABSTRACT

The bottleneck of linearity test for high-resolution ADCs lies in the design and manufacturing of fast and stationary signal generators with performance much better than the specification of ADCs under test. Recently a cost-effective approach was proposed for precision ADC linearity test using low-linearity but easy-to-generate ramp signals. This approach relaxed the linearity requirements on the signal generator and maintained high test accuracy by employing a stimulus error identification and removal algorithm. In this paper, a reduced-density interleaved sampling scheme is proposed for the new approach to cut down the data collection time and guarantee the new approach's robustness to the environmental non-stationarity. Theoretical analyses and simulation results show that with the discussed sampling scheme, the test time of the original approach can be reduced by nearly a factor of two and 16-bit test accuracy can be achieved by using 7-bit linear ramp signals, which is comparable to the performance of the original ADC test approach.

1. INTRODUCTION

DC linearity of analog-to-digital converters (ADCs) has been historically tested by using the histogram method with a ramp or sine-wave as the test signal [1]. To accurately characterize an ADC's linearity, the test signal is required to be much more linear than the ADC under test. As the performance of ADCs continues to improve, linearity test for high resolution and high speed ADCs is becoming more and more a challenging and expensive task. Practical test solutions usually require the test accuracy to remain within 10% of the device specification, so 0.2-least significant bit (LSB) accuracy is required to test an ADC with a specification of 2-LSB integral non-linearity (*INL*) specification. One LSB of a 16-bit ADC with a 2-V supply corresponds to about 30 μV. Achieving a 0.2 LSB (6 μV) source linearity for testing such an ADC is extremely challenging. Moreover, many critical applications require a full code test for an ADC's linearity. The full code test time of a high-resolution ADC often runs in the order of a minute on an expensive mixed-signal automatic test equipment (ATE). Requiring the test signal generator to remain stationary during this long test time creates another challenge for linearity test. So the bottleneck for high-resolution ADC test is how to cost-effectively design and manufacture a fast, stationary and accurate signal generator.

Lots of researches have been done on the ADC test problem. Linear modeling was used to reduce the test complexity and shorten the test time [2]. On chip test functions were designed for built-in self-test (BIST) to replace the expensive external testers [3]. Statistical analysis was incorporated in ADC test to improve the test accuracy [4]. Recently a test approach for precision ADCs using low-linearity ramp signals was proposed in authors' previous work [5]. This approach dramatically relaxed the requirement on the source linearity for ADC test and maintained high accuracy by employing a stimulus error identification and removal (SEIR) algorithm and two non-linear ramp signals with a constant offset as excitations to the ADC under test. If test signals are allowed to be non-linear and there is no predetermined requirement on their characteristics, the signal generator can be more stationary and work faster, which is critical for improving test accuracy and reducing test cost. Furthermore, such a non-linear source can be implemented on chip with a small die area and is suitable for the purpose of BIST.

This paper is looking at practical implementation issues of the SEIR approach proposed in [5]. A reduced-density sampling scheme is proposed to cut down the test time. Interleaved measurements between two test signals are used to cope with the environmental non-stationarity. Using this scheme, the SEIR approach can achieve the same high accuracy in ADC test with significantly shortened test time. Section 2 will briefly review the SEIR approach. The proposed sampling scheme will be discussed in Section 3. Simulation results will be presented in Section 4.

2. A TEST APPROACH FOR PRECISON ADCS USING LOW-LINEARITY RAMP SIGNALS

In this section, mathematical details of the SEIR approach for ADC linearity test will be reviewed. An *n*-bit ADC has

$N=2^n$ distinct output codes. The static input-output characteristic of the ADC can be modeled as

$$D(x)=\begin{cases}0, & x\le T_0,\\ k, & T_{k-1}<x\le T_k,\\ N-1, & T_{N-2}<x,\end{cases} \quad (1)$$

where D is the output code, x is the input voltage, and T_k's are transition points of the ADC. In equation (1), it is assumed that the ADC is monotonic and has no missing code. One of the most widely used linearity metrics for ADCs is the integral non-linearity (*INL*). For each code, an INL_k is defined as

$$INL_k=\frac{T_k-T_0}{T_{N-2}-T_0}(N-2)-k\cdot \quad (2)$$

The *INL* is the maximum magnitude of INL_k's over all k,

$$INL=\max_k\{|\,INL_k\,|\}\cdot \quad (3)$$

A larger *INL* indicates an ADC has larger non-linearity.

A general nonlinear ramp signal can be modeled as

$$x(t)=x_{os}+\eta t+F(t), \quad (4)$$

where x_{os} is a DC offset, η is the slope of the linear component, and $F(t)$ is a non-linear component. Transition time t_k is defined to be the time at which the ramp signal is equal to the k[th] transition point,

$$T_k=x(t_k)\cdot \quad (5)$$

Without affecting the linearity test results, Eq. (4) can be normalized and written as

$$x(t)=t+F(t),\ 0\le t\le 1\cdot \quad (6)$$

If $F(t)$ and t_k are known or measured, T_k, INL_k and an ADC's linearity can be identified by using equations above.

However, $F(t)$ is usually unknown. To identify the ramp nonlinearity, $F(t)$ is expanded over a set of basis function $F_j(t)$'s with coefficient a_j's,

$$F(t)=\sum_{j=1}^{M}a_jF_j(t)\cdot \quad (7)$$

The SEIR algorithm uses two ramp signals with a constant offset to test an ADC,

$$x_1(t)=t+F(t) \quad (8)$$

and $x_2(t)=x_1(t)-\alpha\cdot$ (9)

By feeding the two ramp signals into an ADC under test, we can collect two sets of histogram data $H_{k,1}$'s and $H_{k,2}$'s and get two estimates for a transition point T_k,

$$\hat{T}_{k,1}=\hat{t}_{k,1}+\sum_{j=1}^{M}a_jF_j(\hat{t}_{k,1}) \quad (10)$$

and $\hat{T}_{k,2}=\hat{t}_{k,2}+\sum_{j=1}^{M}a_jF_j(\hat{t}_{k,2})-\alpha,$ (11)

where the transition times are estimated from the histogram data $H_{k,1}$'s and $H_{k,2}$'s as

$$\hat{t}_{k,1}=\sum_{i=1}^{k}H_{i,1}\Big/\sum_{i=1}^{N-2}H_{i,1} \quad (12)$$

and $\hat{t}_{k,2}=\left(-H_{0,1}+\sum_{i=0}^{k}H_{i,2}\right)\Big/\sum_{i=1}^{N-2}H_{i,1}\cdot$ (13)

The estimates in Eq. (10) and (11) have to be the same since they are for the same T_k. By equating them, we have an equation that involves only the ramp non-linearity without any ADC parameters for each code k,

$$\hat{t}_{k,1}+\sum_{j=1}^{M}a_jF_j(\hat{t}_{k,1})=\hat{t}_{k,2}+\sum_{j=1}^{M}a_jF_j(\hat{t}_{k,2})-\alpha. \quad (14)$$

There are totally N-3 equations in Eq. (14) and M+1 unknown variables a_j's and α. N is always much larger than M. For example, N is equal to 65536 for a 16-bit ADC, while M=30 is usually more than enough for testing 16-bit ADCs. Furthermore, Eq. (14) is linear in a_j's and α. We can robustly estimate the unknowns using the standard least squares (LS) method,

$$\{\hat{a}_j's,\hat{\alpha}\}=\arg\min\left\{\sum_{k=1}^{N-3}\left[\hat{t}_{k,1}-\hat{t}_{k,2}+\sum_{j=1}^{M}a_j\left(F_j(\hat{t}_{k,1})-F_j(\hat{t}_{k,2})\right)+\alpha\right]^2\right\}. \quad (15)$$

With the knowledge of ramp nonlinearity a_j's, we can remove their effects on the histogram data and accurately identify an ADC's transition point as

$$\hat{T}_{k,1}=\hat{t}_{k,1}+\sum_{j=1}^{M}\hat{a}_jF_j(\hat{t}_{k,1})\cdot \quad (16)$$

Thus ADC's linearity performance can be determined by using Eq. (2) and (3).

3. A REDUCED-DENSITY INTERLEAVED SAMPLING SCHEME FOR THE SEIR APPROACH

In the previous work, the second test signal is sampled at a same density as the first signal [5]. A more efficient sampling scheme for the second signal will be introduced in this section. It can significantly shorten the test time and suppress the effects of the environmental non-stationarity of the signal generator by appropriately interleaving the measurements between the first and second signals.

3.1. Testing time reduction

The main contribution of the second ramp signal to the SEIR algorithm is providing a second estimate for the transition points as in Eq. (11) to identify the ramp non-

linearity. The samples taken on the second signal are mostly to reduce the effects of the random noise and quantization errors on the transition time estimation. However, there are much more equations in Eq. (14) than the unknown variables, as discussed in Section 2, and the LS method is robust to the noise and quantization effects. Therefore the accuracy of the histogram measurement for the second signal can be significantly reduced by taking fewer samples, which will not affect the ramp non-linearity identification. On the other hand, taking fewer samples on the second ramp signal can dramatically reduce the total test time. For example, if the first signal is sampled at a density of 32 samples per ADC code, a sampling density of 1 sample per code for the second signal can reduce more than 48% of test time as compared to a sampling density of 32 samples per code for the second signal. That means the test time of the SEIR algorithm can be shortened by nearly a factor of two when taking fewer samples on the second signal and get the same performance.

3.2. Environmental nonstationarity compensation

The SEIR algorithm requires the offset between the two signals be a constant to guarantee the ramp non-linearity identification performance. If there is environmental non-stationarity existing, such as temperature-dependent reference voltage drifting, the offset between two signals can change from time to time and make the identified ramp non-linearity different from the true non-linearity. This will cause significant errors in ADC linearity test if the error in ramp identification is larger than 1 LSB. To cope with this non-stationarity issue, the measurements for the two signals will be interleaved instead of taking the measurement of one signal after all the measurements of the other signal are done.

Combining the reduced-density sampling scheme and the interleaved measurements, a triangular wave implementation of the histogram measurement can be depicted as in Figure 1. The first signal is plotted in the blue solid line. The second signal is plotted in the red dashed line. The sampling density for the second signal is 1/8 of the density of the first signal. The measurement for the second signal is interleaved in the middle of the measurements for the first signal. The ADC's input range is from 0 to 1 V. The two signals are appropriately generated so that both of them cover the whole input range and touch all the transition points. When a circuit is working, the temperature of the circuit may keep increasing because of the heat generated and change the reference voltage. Temperature-dependent reference voltage drifting can be mainly modeled as a first order non-stationarity error. By using this interleaving scheme, effects of the first order environmental non-stationarity can be eliminated.

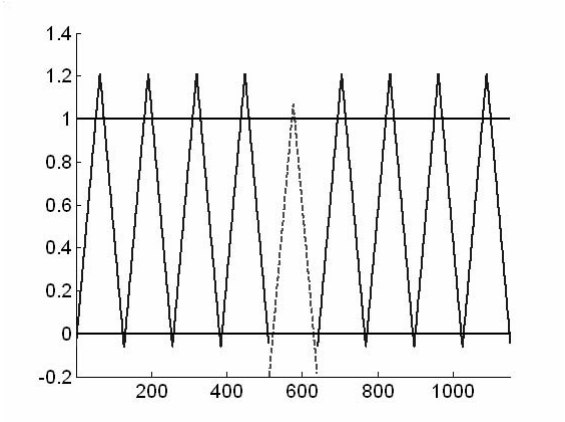

Figure 1 Reduced-density interleaved sampling scheme.

4. SIMULATION RESULTS

Simulations have been done to verify the performance of the reduced-density interleaved sampling scheme. The simulation results generated by using the proposed scheme are compared to the results generated by using a same sampling density for two signals. In simulations, ADCs were modeled by using flash structures with random resistor mismatch errors. Test ramp signals used in simulations were 7-bit linear with a third order polynomial non-linearity. The sampling density for the first signal was fixed at 32 samples per ADC code (SPAC). The additive noise at the ADC's input node had a standard deviation of 0.5 LSB. The offset between the two signals was arbitrarily chosen as 0.2% of the whole input range of the ADC. 32 sinusoidal basis functions were used in the ramp identification. The reference voltage had a linear drift of 1000 ppm over the whole test duration.

Using a sampling density of 1 SPAC for the second signal, the true and estimated INL_k's of a 16-bit ADC are plotted in blue and green on the top of Figure 2, respectively. The two signals were interleaved as shown in Figure 1. The errors in the INL_k estimation, the difference between identified and true values, are plotted in black on the same graph and zoomed in on the bottom of Figure 2. The errors are all below 1 LSB level. That means the ADC test achieved a 16-bit accuracy by using only 7-bit linear signals with the proposed sampling scheme. The estimation results for the same ADC using 32 SPAC for the second signal without interleaved measurements are plotted in Figure 3. There is an error of more than 1500 LSB in INL_k estimation. This error came form the 1000 ppm linear drift in the reference voltage. By comparing the two figures, we can see that the proposed sampling scheme eliminated the effect of the linear reference voltage drift.

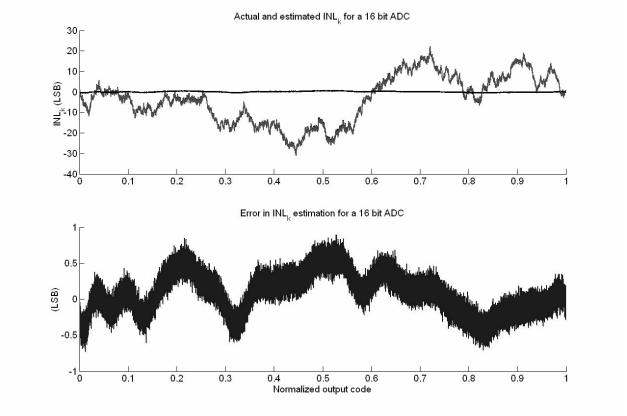

Figure 2 INL_k estimation using 1 SPAC for the 2nd signal with interleaved measurements.

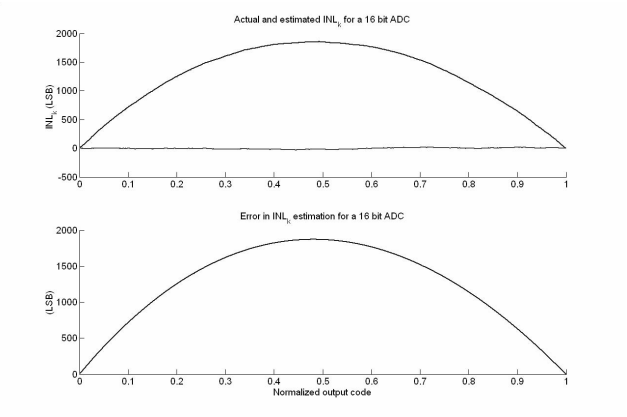

Figure 3 INL_k estimation using 32 SPAC for the 2nd signal without interleaved measurements.

Simulations were done to statistically study the performance of the reduced-density sampling scheme. Figure 4 shows the INL estimation errors for 32 different ADCs using 1 SPAC for the second ramp signal in black circles. All of the INL estimation errors are bellow the 1 LSB level. For comparison, 32 SPAC for the second signal were also used to testing the same set of ADCs and the INL estimation errors are plotted in red diamonds in Figure 4. To make a fair comparison, the reference voltage drifting during the test was compensated for 32 SPAC results by using similar interleaved measurements. The results show that the performance of the 1 SPAC and 32 SPAC test scheme were comparable to each other, both with errors less than 1 LSB.

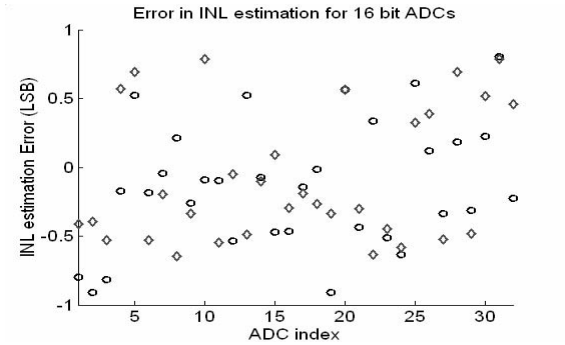

Figure 4 Error in *INL* estimation for 32 16-bit ADCs

5. CONCLUSIONS

A reduced-density interleaved sampling scheme for a high precision ADC linearity test approach using low-linearity ramp signals is presented. The introduced sampling scheme can significantly reduce the test time for high precision ADCs by nearly a factor of two and it is robust to common environmental non-stationarity. 16-bit test accuracy was achieved in simulations by using only 7-bit linear ramp signals, with 1000 ppm reference voltage drifting over the total test duration. This sampling scheme can be used in linearity test for high-resolution and high-speed ADCs together with the cost-effective SEIR algorithm to further cut down the test time and the test cost. It is especially useful for on chip test where a temperature oven or other environmental stabilization mechanisms are usually not available. Other interleaving sequences can be developed to eliminate the effects of more complex environmental non-stationarity errors based on this scheme.

6. REFERENCES

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